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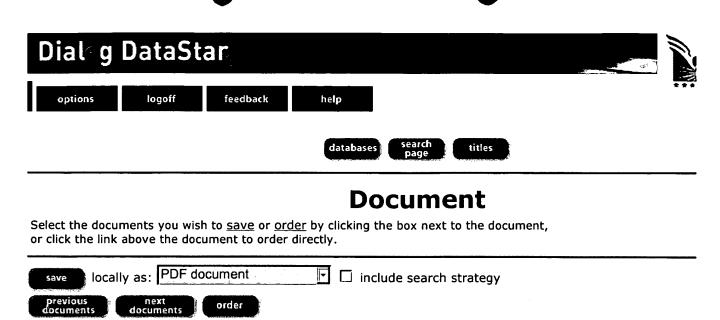
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INSPEC - 1969 to date (INZZ)

Accession number & update
    5507381, C9704-1180-024; 970304.
Title
    Divide-and-conquer techniques for global throughput optimization.
Author(s)
    Guerra-L; Potkonjak-M; Rabaey-J; Ed. by Burleson-W; Konstantinides-K; Meng-T.
Author affiliation
    Dept of Electr Eng & Comput Sci, California Univ, Berkeley, CA, USA.
Source
    VLSI Signal Processing, IX, San Francisco, CA, USA, 30 Oct.-1 Nov. 1996.
    Sponsors: IEEE Signal Process. Soc.
    In: p.137-46, 1996.
ISSN
    ISBN: 0-7803-3134-6, CCCC: 0 7803 3134 6/96/ ($5.00).
Publication year
    1996.
Language
    EN.
Publication type
    CPP Conference Paper.
Treatment codes
    T Theoretical or Mathematical.
Abstract
    The paper proposes a divide-and-conquer approach for global throughput optimization designed to coordinate existing techniques and enable their more effective use. The "divide" approach consists of **logical partitioning** of the computation into subparts. The techniques for **partitioning** the computation, and the corresponding scheme for classifying the subparts is presented. The subparts are optimized or "conquered" through coordinated application of existing optimization techniques. Optimization techniques that are effective for each class have been characterized in terms of their expected effect on throughput. The approach is not limited to a specific class of computations and gives higher, or at least equal, improvement than previously reported techniques on all examples. (13 refs).
Descriptors
    divide-and-conquer-methods; optimisation.
Keywords
    divide and conquer techniques; global throughput optimization; **logical** computation **partitioning;**

subpart classification; coordinated optimization techniques.

Classification codes

C1180 (Optimisation techniques).
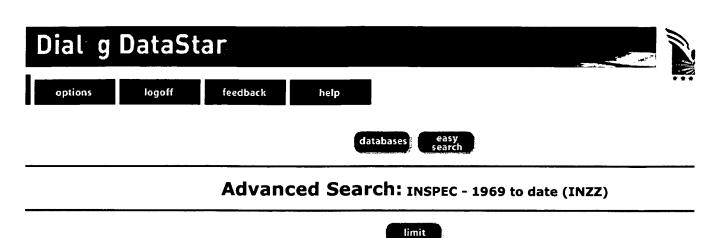
C1230 (Artificial intelligence).

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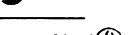- account info
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related people   E. Crawley
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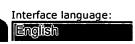
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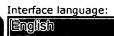| Basic Search | Advanced Search | Topic Guide | Publication Search | Marked List : 0 articles | Interface language: English |

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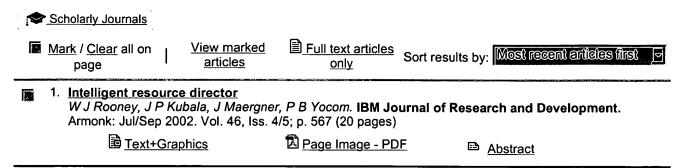| Basic Search | Advanced Search | Topic Guide | Publication Search | Marked List : 0 articles | Interface language: English |

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W J Rooney, J P Kubala, J Maergner, P B Yocom. **IBM Journal of Research and Development.**
Armonk: Jul/Sep 2002. Vol. 46, Iss. 4/5; p. 567 (20 pages)

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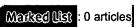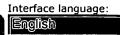
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ALAN ZEICHICK. **InternetWeek.** Manhasset: Sep 25, 2000. p. PG.61

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▮ 2. **IBM bolsters manageability of clustered S80 servers**
Martin J Garvey. **InformationWeek.** Manhasset: Sep 11, 2000. p. 32 (1 page)

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▮ 3. **Vision Releases Object Mirroring System R7.0; Award Winning OMS/400 Poised to Become the De-Facto Standard in AS/400 Data Mirroring**
Business Editors and High-Tech Writers. **Business Wire.** New York: Sep 6, 2000. p. 1

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▮ 4. **Partition Magic 5**
Ron LaFon. **CADalyst.** Eugene: Sep 2000. Vol. 17, Iss. 9; p. 32 (1 page)

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▮ 5. **Intelligent Agents for ATM Network Control and Resource Management: Experiences and Results from an Implementation on a Network Testbed**
E. Vayias, J. Soldatos, J. Bigham, L. Cuthbert, Z. Luo. **Journal of Network and Systems Management.** New York: Sep 2000. Vol. 8, Iss. 3; p. 373

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▮ 6. **AS/400 leads the league in Java performance; IBM's AS/400 server rocks the house in two Java benchmarks**
John Carr, InfoWorld Test Center. **JavaWorld.** San Francisco: Aug 15, 2000. p. 1

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▮ 7. **AS/400 leads the league in Java performance**
John Carr. **InfoWorld.** San Mateo: Jul 31, 2000. Vol. 22, Iss. 31; p. 56 (1 page)

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▮ 8. **Changing perceptions: IBM's AS/400 morphs into powerful, dynamic e-business server**
Maggie Biggs. **InfoWorld.** San Mateo: Jul 31, 2000. Vol. 22, Iss. 31; p. 59 (1 page)

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9. **Latest OS/400 bolsters e-business**
   Tim Fielden. **InfoWorld.** San Mateo: Jul 31, 2000. Vol. 22, Iss. 31; p. 50 (2 pages)

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10. **ENVISION integrates online, near online, and offline storage**
    Glenn Jacobsen. **Computer Technology Review.** Los Angeles: Jul 2000. Vol. 20, Iss. 7; p. 42 (2 pages)

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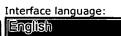
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3. **An approach to organizing a management accounting curriculum**
   Peter C Brewer. **Issues in Accounting Education.** Sarasota: May 2000. Vol. 15, Iss. 2; p. 211 (25 pages)
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4. **TrueSAN Networks Launches First LUN Masking Technology for Fibre Channel SANs; Delivers SANengage Technology for Enterprise-wide Data Consolidation and Asset Protection**
   Business Editors/High Tech Writers. **Business Wire.** New York: Sep 14, 1999. p. 1
   Full text | Abstract

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5. **Exploiting the benefits of Y2K preparation**
   Stewart Robertson, Philip Powell. **Association for Computing Machinery. Communications of the ACM.** New York: Sep 1999. Vol. 42, Iss. 9; p. 42 (7 pages)
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6. **FIFOs excel at matching frequencies, buses, and data rates**
   Stuart Speed, Mark Baumann. **Electronic Design.** Cleveland: Aug 9, 1999. Vol. 47, Iss. 16; p. 77 (4 pages)
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7. **Figuring out reconfigurable logic**
   Brian Dipert. **EDN.** Boston: Aug 5, 1999. Vol. 44, Iss. 16; p. 103 (7 pages)
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8. **Open file systems with Solaris**
   Paul A Watters. **Inside Solaris.** Louisville: Jun 1999. Vol. 5, Iss. 6; p. 5 (5 pages)
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9. **Hitachi Data Systems Introduces the World's Most Powerful CMOS- based Servers Designed to Exploit the Web's Capacity for E-commerce**
Business Editors & High Tech Writers. **Business Wire.** New York: May 17, 1999. p. 1
📄 Full text   📖 Abstract

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10. **SANs offer solution to data interoperability problems**
Christopher Stakutis. **HP Chronicle.** Austin: Apr 1999. Vol. 16, Iss. 5; p. 10 (1 page)
📄 Full text   📰 Page Image - PDF   📖 Abstract

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1. **Server partitioning**
   Jaikumar Vijayan. **Computerworld.** Framingham: Mar 6, 2000. Vol. 34, Iss. 10; p. 74 (1 page)

   Text+Graphics   Page Image - PDF   Abstract

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2. **Garbage collecting the Internet: A survey of distributed garbage collection**
   Saleh E Abdullahi, Graem A Ringwood. **ACM Computing Surveys.** Baltimore: Sep 1998. Vol. 30, Iss. 3; p. 330 (44 pages)

   Text+Graphics   Page Image - PDF   Abstract

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3. **Circuit design techniques for the high-performance CMOS IBM S/390 Parallel Enterprise Server G4 microprocessor**
   L Sigal, J D Warnock, B W Curran, Y H Chan, et al. **IBM Journal of Research and Development.** Armonk: Jul-Sep 1997. Vol. 41, Iss. 4/5; p. 489 (15 pages)

   Text+Graphics   Page Image - PDF   Abstract

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4. **Client server computing**
   The Hindu. Madras: Mar 7, 1996. p. NOPGCIT

   Full text   Abstract

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5. **RTL floor planning set to drive synthesis**
   Rod Dudzinski, Director of Design Tools Marketing, Compass Design Automation, San Jose, Calif.. **Electronic Engineering Times.** Manhasset: Nov 27, 1995. p. 52

   Full text   Citation

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6. **SNMP scaffolding**
   Coopee, Todd. **Network World.** Framingham: Feb 6, 1995. Vol. 12, Iss. 6; p. 33 (2 pages)

   Full text   Page Image - PDF   Abstract

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7. **Practical considerations for network addressing using CIDR**
   Eidnes, Havard. **Association for Computing Machinery. Communications of the ACM.** New York: Aug 1994. Vol. 37, Iss. 8; p. 46 (8 pages)

   Full text   Page Image - PDF   Abstract

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8. **A powerful architecture for enterprise networking**
   Bryenton, Alan, Shew, Stephen. **Telesis.** Ottawa: May 1994. p. 68 (11 pages)

   Full text   Abstract

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9. **Amdahl debuts new 5995M processors, including largest capacity models in the System/390 marketplace**
   Stewart, William. **Business Wire.** New York: Mar 29, 1994. p. 1

   📄 Full text   ▣ Abstract

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10. **Sharing Systems**
    Anonymous. **Capacity Management Review.** Naples: Apr 1991. Vol. 19, Iss. 4; p. 7 (2 pages)

    📄 Full text   📄 Page Image - PDF   ▣ Abstract

1-10 of 10

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1. **Cisco, IBM to enhance cluser load balancing**
   Jim Duffy. **Network World.** Framingham: Sep 11, 2000. Vol. 17, Iss. 37; p. 14 (1 page)

   Full text   Page Image - PDF   Citation

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2. **Big Blue boosts mainframe management**
   Marc Songini. **Network World.** Framingham: Sep 4, 2000. Vol. 17, Iss. 36; p. 10 (1 page)

   Full text   Page Image - PDF   Abstract

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3. **IBM: IBM expands e-business options for enterprise customers; S/390 server platform enhancements accelerate web-enablement, integration; [1]**
   M2 Presswire. Coventry: Mar 8, 2000. p. 1

   Full text   Abstract

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4. **IBM: IBM expands e-business options for enterprise customers; S/390 server platform enhancements accelerate web-enablement, integration**
   M2 Presswire. Coventry: Mar 8, 2000. p. 1

   Full text   Citation

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5. **Server partitioning**
   Jaikumar Vijayan. **Computerworld.** Framingham: Mar 6, 2000. Vol. 34, Iss. 10; p. 74 (1 page)

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6. **IBM: IBM expands e-business options for enterprise customers S/390 server platform enhancements accelerate web-enablement, integration; [1]**
   M2 Presswire. Coventry: Mar 3, 2000. p. 1

   Full text   Abstract

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7. **IBM: IBM expands e-business options for enterprise customers S/390 server platform enhancements accelerate web-enablement, integration**
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8. **The next logical step**
   Edward F Moltzen. **CRN.** Jericho: Dec 13, 1999. p. 109 (1 page)

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9. **On its own merits**

Roberto Michel. **MSI.** Oak Brook: Jun 1999. p. R2 (6 pages)

  📄 Text+Graphics   📄 Page Image - PDF   📧 Citation

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10. **Big Blue bolsters front-end processor**
    Marc Songini. **Network World.** Framingham: Mar 15, 1999. Vol. 16, Iss. 11; p. 8 (1 page)

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1-10 of 21   < First | < Previous   1 2 3   Next >

                                                  Results per page: 10

Basic Search   Tools: Search Tips   Browse Topics   13 Recent Searches

LPAR AND IBM   [Search] [Clear]

Database: Multiple databases   Select multiple databases

Date range: Before this date...   mm/dd/yyyy   About

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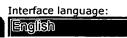
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Basic Search

Tools: Search Tips   Browse Topics   5 Recent Searches

(LPAR AND (OS?400) AND (v4r4))   Search   Clear

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Basic Search

Tools: Search Tips   Browse Topics   6 Recent Searches

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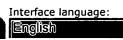
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Tools: Search Tips   Browse Topics   3 Recent Searches

(LPAR OR (logic* partition*)) AND (dedicat* processor*) AND (shar* proces| Search   Clear

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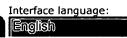
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■ 1. **Two innovators support multiple platforms to earn enterprise developments award**
   Maggie Biggs. **InfoWorld.** San Mateo: Jan 17, 2000. Vol. 22, Iss. 3; p. 70 (1 page)
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■ 2. **Executive briefing: Hitachi bipolar mainframes battle for future markets**
   Anonymous. **Computer Economics Report.** Carlsbad: Oct 1998. Vol. 20, Iss. 10; p. 4 (3 pages)
   🖹 Text+Graphics   🔁 Page Image - PDF   🖹 Abstract

■ 3. **On the path to the I2O architecture**
   Borkar, Paresh, Wilson, Jeanette. **Computer Technology Review.** Los Angeles: Feb 1997. Vol. 17, Iss. 2; p. 20 (2 pages)
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Basic Search

Tools: Search Tips   Browse Topics   4 Recent Searches

(LPAR OR (logic* partition*)) AND (dedicat* processor*)   [Search] [Clear]

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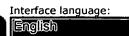| Basic Search | Advanced Search | Topic Guide | Publication Search | Marked List : 0 articles | Interface language: English |

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▣ 1. **Desktop Hyper-Threading - Coming Soon! ; Intel's Hyper-Threading technology will soon be available for desktop PCs using the upcoming 3.06GHz P4 chip. How does Hyper- Threading work, and will it matter in your computing future? Nick provides an in-depth technology inspection and update.**
Nick Stam. **ExtremeTech.com.** New York: Oct 3, 2002. p. 1

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1 **MIBlet, logically partitioned resource controller, in SNMP/SMI and C(**
for open switching architecture
Jai-Jin Lim; In-Tae Ryoo; Kyung Hee;
High Performance Switching and Routing, 2000. ATM 2000. Proceedings of the
Conference on , 26-29 June 2000
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1   **A scheduling and pipelining algorithm for hardware/software system**
Bakshi, S.; Gajski, D.D.;
System Synthesis, 1997. Proceedings., Tenth International Symposium on , 17
Sept. 1997
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2   **Parallel simulation of VHDL-AMS models**
Hirsch, H.; Chawla, P.; Carter, H.W.;
Aerospace and Electronics Conference, 1998. NAECON 1998. Proceedings of the
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Results:
Journal or Magazine = **JNL**   Conference = **CNF**   Standard = **STD**

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1 **Energy/power estimation of regular processor arrays**
Derrien, S.; Rajopadhye, S.;
System Synthesis, 2002. 15th International Symposium on , 2-4 Oct. 2002
Page(s): 50 -55

[Abstract]   [PDF Full-Text (529 KB)] **IEEE CNF**

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2 **Register aware scheduling for distributed cache clustered architectui**
Zhong Wang; Xiaobo Sharon Hu; Sha, E.H.-M.;
Design Automation Conference, 2003. Proceedings of the ASP-DAC 2003. Asia i
South Pacific , 21-24 Jan. 2003
Page(s): 71 -76

[Abstract]   [PDF Full-Text (764 KB)] **IEEE CNF**

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3 **SID: synthesis of integral design**
Hooper, D.F., Jr.;
Computer Design: VLSI in Computers and Processors, 1988. ICCD '88., Proceei
the 1988 IEEE International Conference on , 3-5 Oct. 1988
Page(s): 204 -208

[Abstract]   [PDF Full-Text (316 KB)] **IEEE CNF**

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4 **Placement-based partitioning for lookup-table-based FPGAs**
Trimberger, S.; Chene, M.-R.;
Computer Design: VLSI in Computers and Processors, 1992. ICCD '92. Proceed
IEEE 1992 International Conference on , 11-14 Oct. 1992

Page(s): 91 -94

[Abstract]   [PDF Full-Text (308 KB)] **IEEE CNF**

5 **Synthesis of throughput-optimized multichip architectures**
Gebotys, C.H.;
Custom Integrated Circuits Conference, 1993., Proceedings of the IEEE 1993 ,
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[Abstract]   [PDF Full-Text (428 KB)] **IEEE CNF**

6 **A unified systolic design technique based on integral matrix theory**
Lorenzelli, F.; Yao, K.;
VLSI Signal Processing, VI, 1993., [Workshop on] , 20-22 Oct. 1993
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[Abstract]   [PDF Full-Text (412 KB)] **IEEE CNF**

7 **A parallel force direct based VLSI standard cell placement algorithm**
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Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium o
May 1993
Page(s): 2071 -2074 vol.3

[Abstract]   [PDF Full-Text (344 KB)] **IEEE CNF**

8 **Pipelined fault simulation on parallel machines using the circuit flow**

Tai, S.-E.; Bhattacharya, D.;
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1993 IEEE International Conference on , 3-6 Oct. 1993
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[Abstract]   [PDF Full-Text (352 KB)] **IEEE CNF**

9 **The PowerPC 601 design methodology**
Brodnax, T.; Schiffli, M.; Watson, F.;
Computer Design: VLSI in Computers and Processors, 1993. ICCD '93. Proceed
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Page(s): 248 -252

[Abstract]   [PDF Full-Text (480 KB)] **IEEE CNF**

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10 **Development of parallelism for circuit simulation by tearing**
Onozuka, H.; Kanoh, M.; Mizuta, C.; Nakata, T.; Tanabe, N.;
Design Automation, 1993, with the European Event in ASIC Design. Proceeding
European Conference on , 22-25 Feb. 1993
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11 **Methods for retargetable DSP code generation**
Leupers, R.; Niemann, R.; Marwedel, P.;
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12 **The scalability of linear filters on hypercube concurrent computers**
Dick, C.H.;
Signals, Systems and Computers, 1994. 1994 Conference Record of the Twenty
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[Abstract]   [PDF Full-Text (340 KB)] **IEEE CNF**

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13 **An automated design process for the CHAMP module**
Patriquin, R.; Gurevich, I.;
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14 **Parallel logic simulation on a workstation cluster**
Murakami, T.; Wada, K.; Okano, S.;
Communications, Computers, and Signal Processing, 1995. Proceedings. IEEE F
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Page(s): 268 -271

[Abstract]   [PDF Full-Text (292 KB)] **IEEE CNF**

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15 **Adaptation of force-directed scheduling algorithm for hardware/sof partitioning**
Rousseau, F.; Benzakki, J.; Berge, J.-M.; Israel, M.;
Rapid System Prototyping, 1995. Proceedings., Sixth IEEE International Worksh on , 7-9 June 1995
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[Abstract]   [PDF Full-Text (376 KB)] **IEEE CNF**

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16 **Proceedings of the 8th International Conference on VLSI Design**
VLSI Design, 1995., Proceedings of the 8th International Conference on , 4-7 J; 1995

[Abstract]   [PDF Full-Text (1460 KB)] **IEEE CNF**

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17 **Data parallel fault simulation**
Amin, M.B.; Vinnakota, B.;
Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proceed 1995 IEEE International Conference on , 2-4 Oct. 1995
Page(s): 610 -615

[Abstract]   [PDF Full-Text (608 KB)] **IEEE CNF**

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18 **A parallel algorithm for fault simulation based on PROOFS**
Parkes, S.; Banerjee, P.; Patel, J.;
Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proceed 1995 IEEE International Conference on , 2-4 Oct. 1995
Page(s): 616 -621

[Abstract]   [PDF Full-Text (516 KB)] **IEEE CNF**

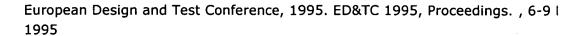19 **Rapid prototype of a hardware emulator for a SIMD processor array**
Andrews, D.L.; Wheeler, A.; Wealand, B.; Kancler, C.;
European Design and Test Conference, 1995. ED&TC 1995, Proceedings. , 6-9 I 1995
Page(s): 391 -396

[Abstract]   [PDF Full-Text (560 KB)] **IEEE CNF**

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20 **Proceedings the European Design and Test Conference. ED&TC 1995**

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[Abstract]   [PDF Full-Text (24 KB)] **IEEE CNF**

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21 **An improved cost function for static partitioning of parallel circuit
simulations using a conservative synchronization protocol**
Kapp, K.L.; Hartrum, T.C.; Wailes, T.S.;
Parallel and Distributed Simulation, 1995. (PADS'95), Proceedings., Ninth Work
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[Abstract]   [PDF Full-Text (712 KB)] **IEEE CNF**

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22 **Fault location based on circuit partitioning**
Pomeranz, I.; Reddy, S.M.;
Computer Design: VLSI in Computers and Processors, 1996. ICCD '96. Proceed
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23 **A hardware/software partitioning algorithm for designing pipelined
with least gate counts**
Nguyen Ngoc Binh; Imai, M.; Shiomi, A.; Hikichi, N.;
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24 **The design of mixed hardware/software systems**
Adams, J.K.; Thomas, D.E.;
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25 **Acceleration of mincut partitioning using hardware CAD accelerator
TP5000**
Sano, M.; Shimogori, S.; Hirose, F.;
Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia anc
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1 Decay-usage scheduling in multiprocessors

D. H. J. Epema
November 1998 **ACM Transactions on Computer Systems (TOCS)**, Volume 16 Issue 4

Full text available: ▣ pdf(377.13 KB)   Additional Information: full citation, abstract, references, index terms

Decay-usage scheduling is a priority-aging time-sharing scheduling policy capable of dealing with a workload of both interactive and batch jobs by decreasing the priority of a job when it acquires CPU time, and by increasing its priority when it does not use the (a) CPU. In this article we deal with a decay-usage scheduling policy in multiprocessors modeled after widely used systems. The priority of a job consists of a base priority and a time-dependent component based on processor usage. B ...

Keywords: control, convergence, decay usage, priorities, shares

2 The impact of distributions and disciplines on multiple processor systems

Charles H. Sauer, K. Mani Chandy
January 1979 **Communications of the ACM**, Volume 22 Issue 1

Full text available: ▣ pdf(960.58 KB)   Additional Information: full citation, abstract, references, citings

Simple queueing models are used to study the performance tradeoffs of multiple processor systems. Issues considered include the impact of CPU service disciplines and distributions, level of multiprogramming, multitasking, and job priorities.

Keywords: multiprocessing, multiprogramming, performance evaluation, queueing models, scheduling disciplines

3 An interactive molecular graphics system with a satellite terminal closely coupled to its host

J. D. Foley, W. V. Wright
January 1975 **Proceedings of the 1975 annual conference**

Full text available: ▣ pdf(115.84 KB)   Additional Information: full citation, abstract, index terms

GRIP is an experimental interactive computer graphics system being developed at the University of North Carolina for displaying, evaluating and manipulating models of complex molecular structures. The system displays a molecule as a network of line segments

representing the locations and orientations of the atoms and valence bonds in the structure. It can also display electron-density data (obtained by crystallographic methods) as a three-dimensional contour map. The user can command the sy ...

4 A Level Algorithm for Preemptive Scheduling

Edward C. Horvath, Shui Lam, Ravi Sethi
January 1977 **Journal of the ACM (JACM)**, Volume 24 Issue 1

Full text available: pdf(698.78 KB)   Additional Information: full citation, abstract, references, citings, index terms

Muntz and Coffman give a level algorithm that constructs optimal preemptive schedules on identical processors when the task system is a tree or when there are only two processors available. Their algorithm is adapted here to handle processors of different speeds. The new algorithm is optimal for independent tasks on any number of processors and for arbitrary task systems on two processors, but not on three or more processors, even for trees. By taking the algorithm as a heuristic on

5 Performance modeling of multiprocessor implementations of protocols

Mats Björkman, Per Gunningberg
June 1998 **IEEE/ACM Transactions on Networking (TON)**, Volume 6 Issue 3

Full text available: pdf(285.80 KB)   Additional Information: full citation, references, citings, index terms, review

Keywords: multiprocessor, parallel communication protocols, performance modeling, queueing network model

6 VM-based shared memory on low-latency, remote-memory-access networks

Leonidas Kontothanassis, Galen Hunt, Robert Stets, Nikolaos Hardavellas, Michał Cierniak, Srinivasan Parthasarathy, Wagner Meira, Sandhya Dwarkadas, Michael Scott
May 1997 **ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture**, Volume 25 Issue 2

Full text available: pdf(1.96 MB)   Additional Information: full citation, abstract, references, citings, index terms

Recent technological advances have produced network interfaces that provide users with very low-latency access to the memory of remote machines. We examine the impact of such networks on the implementation and performance of software DSM. Specifically, we compare two DSM systems---Cashmere and TreadMarks---on a 32-processor DEC Alpha cluster connected by a Memory Channel network.Both Cashmere and TreadMarks use virtual memory to maintain coherence on pages, and both use lazy, multi-writer releas ...

7 Interface co-synthesis techniques for embedded systems

Pai Chou, Ross B. Ortega, Gaetano Borriello
December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(175.83 KB)   Additional Information: full citation, abstract, references, citings, index terms
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Abstract: A key aspect of the synthesis of embedded systems is the automatic integration of system components. This entails the derivation of both the hardware and software interfaces that will bind these elements together and permit them to communicate correctly and efficiently. Without the automatic synthesis of these interfaces, designers are not able to fully simulate and evaluate their systems. Frequently, they are discouraged from exploring the design space of different hardware/software p ...

Keywords: CAD, computer interfaces, design cycle, design space exploration tools, embedded systems, glue logic, hardware/software interfaces, real-time systems, synthesis

8 Locking effects in multiprocessor implementations of protocols

Mats Björkman, Per Gunningberg

October 1993 **ACM SIGCOMM Computer Communication Review , Conference proceedings on Communications architectures, protocols and applications**, Volume 23 Issue 4

Full text available: pdf(1.06 MB)   Additional Information: full citation, references, citings, index terms, review

9 A dynamic processor allocation policy for multiprogrammed shared-memory multiprocessors

Cathy McCann, Raj Vaswani, John Zahorjan

May 1993 **ACM Transactions on Computer Systems (TOCS)**, Volume 11 Issue 2

Full text available: pdf(2.26 MB)   Additional Information: full citation, abstract, references, citings, index terms

We propose and evaluate empirically the performance of a dynamic processor-scheduling policy for multiprogrammed shared-memory multiprocessors. The policy is dynamic in that it reallocates processors from one parallel job to another based on the currently realized parallelism of those jobs. The policy is suitable for implementation in production systems in that: —It interacts well with very efficient user-level thread packages, leaving to them many low-level thr ...

Keywords: shared memory parallel processors, threads, two-level scheduling

10 Communication based logic partitioning

Mark Beardslee, Bill Lin, Alberto Sangiovanni-Vincentelli

November 1992 **Proceedings of the conference on European design automation**

Full text available: pdf(715.28 KB)   Additional Information: full citation, references, citings, index terms

11 Logic partitioning—component assignment

Hildegard A. Nidecker, William F. Simon

January 1968 **Proceedings of the 1968 23rd ACM national conference**

Full text available: pdf(752.93 KB)   Additional Information: full citation, abstract, references, citings, index terms

A technique for partitioning logic into groups having minimal interconnection was considered an important tool necessary to the building of the Univac @@@@ 9200 System. Not only would costs be reduced by minimization of the total number of printed circuit assemblies and the total number of backboard connections, but logic signal propogation delay would also be minimized. The price to be paid for these advantages—a multiplicity of unique card types—was fully recognized, but consi ...

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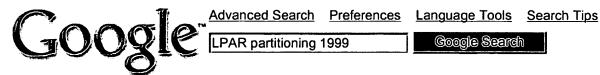| LPAR OS/400 (V4R4 OR V4R5) | Google Search | Search within results

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